EE 330 HW 15 Solutions Spring 2024

Problem 1 Assume C_{REF}=4fF.

$$t_{PROP}=t_{REF}\sum_{i=1}^{3}\frac{FI_{i+1}}{OD_i} \qquad FI_2=3\bullet\frac{3+k}{4}\bigg|_{k=3}=\frac{9}{2} \qquad FI_3=\frac{1+3k}{4}\bigg|_{k=2}=\frac{7}{4} \qquad FI_4=\frac{10fF}{4fF}\bigg|_{k=2}=\frac{5}{2} \qquad OD_1=1 \quad OD_2=3 \quad OD_3=1$$

$$t_{PROP}=t_{REF}\left(\frac{9}{2}+\frac{1}{3}\bullet\frac{7}{4}+\frac{5}{2}\right)=7.6t_{REF}$$

2. Assume ref inverter has $L_{min}=0.6\mu$, $W_{min}=0.9\mu$

a) For 3-input NAND $W_n = n\cdot OD\cdot W_{min} = 3\cdot 4\cdot W_{min} = 10.8\mu$

$W_p = 3\cdot OD\cdot W_{min} = 3\cdot 4\cdot W_{min} = 10.8\mu$

2-input NOR $W_n = OD\cdot W_{min} = 6W_{min} = 5.4\mu$

$W_p = 3\cdot n\cdot OD\cdot W_{min} = 3\cdot 2\cdot 6\, W_{min} = 32.4\mu$

b) with this sizing

$$t_{PROP}(B-K) = t_{REF}\sum_{k=1}^{3}\frac{F_i(k+1)}{OD_k} = t_{PROP}\left(\frac{6+1+6\cdot 7/4}{4}+\frac{3}{6}+\frac{\frac{20}{4}}{3}\right)$$

$$= 6.54\, t_{REF}$$

with minimum sizing

$$t_{PROP}(B-K) = \frac{t_{REF}}{2}\sum_{k=1}^{3}F_i(k+1)\left(\frac{1}{OD_{HLK}}+\frac{1}{OD_{LHK}}\right)$$

$$= \frac{t_{REF}}{2}\left(\frac{3}{2}\left[\frac{1}{1/3}+\frac{1}{1/3}\right]+\frac{1}{2}\left[\frac{1}{1}+\frac{1}{1/6}\right]+\frac{20}{4}\left[\frac{1}{1}+\frac{1}{1/3}\right]\right)$$

$$= \frac{t_{REF}}{2}\left(9+7/2+20\right) = 16.25\, t_{REF}$$

3 a) $$t_{PROP}(A-F) = t_{REF}\sum_{k=1}^{3}\frac{F_i(k+1)}{OD_k}$$

$$= t_{REF}\left(\frac{\left[1+\frac{5}{4}+3\cdot\frac{13}{4}\right]}{1}+\frac{\left[\frac{7}{4}+4\cdot\frac{6}{4}\right]}{3}+\frac{\left[7+\frac{5}{4}+2\cdot\frac{10}{4}\right]}{1}\right)$$

$$= t_{REF}(12+2.58+13.25) = 27.8\, t_{REF}$$

b) Since inverter changes only on HL transitions $f_{TOGGLE} = \frac{400MHz}{2} = 200MHz$

$$P_{DYNAMIC} = f_{TOGGLE}\, C_L V_{DD}^2 = (200E6)\left(3\cdot\frac{5}{4}\cdot 4fF\right)(4v)^2 = 48\mu W$$

c) $$t_{PROP}(A-F) = \frac{t_{REF}}{2}\sum_{k=1}^{3}F_i(k+1)\left(\frac{1}{OD_{HLK}}+\frac{1}{OD_{LHK}}\right)$$

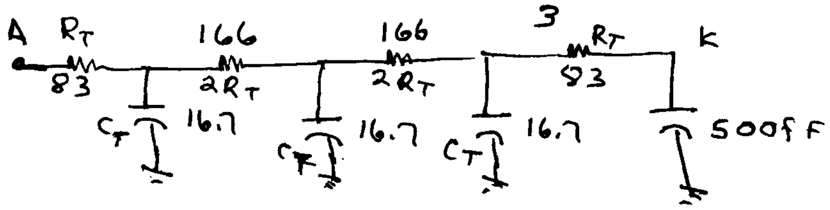
$$= \frac{t_{REF}}{2}\left(\frac{3}{2}\left[\frac{1}{1}+\frac{1}{1/6}\right]+2\left[\frac{1}{1}+\frac{1}{1/12}\right]+\frac{3}{2}\left[\frac{1}{1}+\frac{1}{1/6}\right]\right)$$

$$= \frac{t_{REF}}{2}\left(\frac{21}{2}+26+\frac{21}{2}\right) = 23.5\, t_{REF}$$

4) a) $R_T = R_\square \frac{L}{W}\left(\frac{1}{2n}\right) = (20)\left(\frac{50}{2}\right)\left(\frac{1}{6}\right) = 83.3\,\Omega$

$C_T = \frac{C_d\ W \cdot L}{n} = \frac{.5\,\frac{fF}{\mu^2}\ 100\mu^2}{3} = 16.7\,fF$

b)



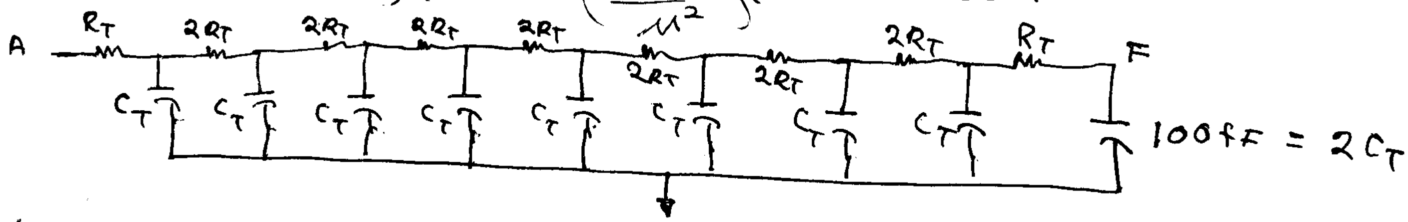
$t_{delay} = R_T C_T + 3R_T C_T + 5R_T C_T + 6R_T(500\,fF)$

$= 9R_T C_T + 6R_T(500\,fF)$

$= (83.3)(9 \cdot 16.7\,fF + 3\,pf) = 262\,psec$

5) $R_T = R_\square\left(\frac{50}{2}\right)\left(\frac{1}{2}\right) = (20)\left(\frac{50}{4}\right)\Omega = 250\,\Omega$

$C_T = (C_d)(2 \cdot 50) = \left(\frac{.5\,fF}{\mu^2}\right)(100\mu^2) = 50\,fF$

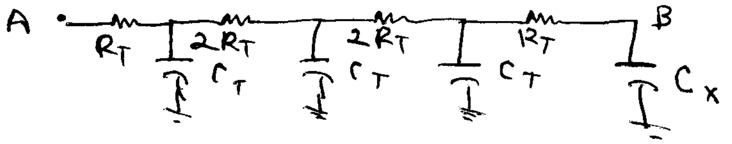


$t_{delay} = R_T C_T + 3R_T C_T + 5R_T C_T + 7R_T C_T + 9R_T C_T + 11R_T C_T + 13R_T C_T$
$+ 15R_T C_T + 16R_T(100\,fF)$

$= R_T(1+3+5+7+9+11+13+15+32)C_T$

$= 96R_T C_T = 1.2\,nsec$

6) a) Consider poly interconnect, use 3-seg model, Assume $C_{REF} = 4fF$



$R_T = R_\square \cdot \frac{L}{W} \cdot \frac{1}{2n} = \frac{50 \cdot 400}{6} = 3.3\,K\Omega$

$C_T = \left(800\,\frac{af}{\mu^2}\right)\left(\frac{400\mu^2}{3}\right) = 107\,fF$

$C_x = C_{REF} \cdot \frac{7}{4} = 7\,fF$

$\therefore t_{AB} = R_T C_T + 3R_T C_T + 5R_T C_T + 6R_T C_x$

$= R_T(9C_T + 6C_x) = 3.3\,nsec$

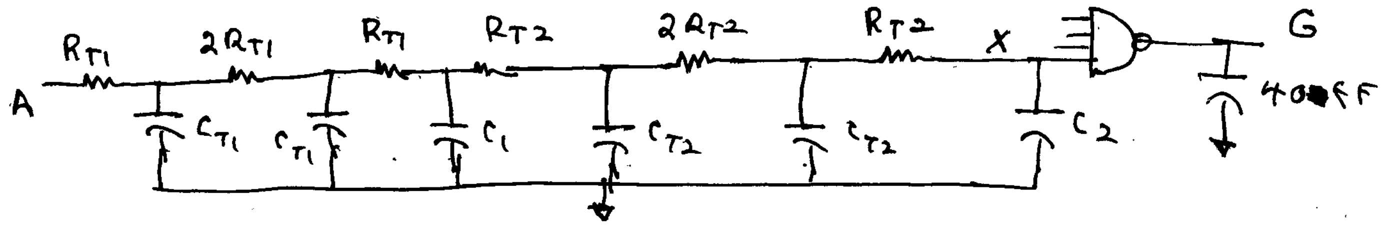
$t_{EF} = \frac{t_{REF}}{2}\sum_{k=1}^{2} F_i(k+1) \underset{t_{REF} = 20\,psec}{=} (10\,psec)\left(1 + \frac{7}{4}\right) = 27.5\,psec$

Thus, the F input will rise first.

b) $t_{PROP} = t_{REF}\sum_{k=1}^{3} F_i(k+1) = t_{REF}\left(1 + \frac{7}{4} + 4\right) \le 6.75\,t_{REF} = 135\,psec$

7) will use 2-segment delay model for each resistor segment

Note: Propagation delay in interconnect is double t_{HL} of interconnect



$$C_1 = (6)\left(\frac{3k+1}{4}\right)\bigg|_{k=2} = \frac{42}{4} C_{REF} = 42fF$$

$$C_2 = \frac{3+k}{4}\bigg|_{k=4} = \frac{7}{4} C_{REF} = 7fF$$

$$R_{T1} = (20\Omega/\square)\left(\frac{20}{2}\right)\left(\frac{1}{4}\right) = 50\Omega \qquad R_{T2} = \left(40\frac{\Omega}{\square}\right)\left(\frac{20}{2}\right)\left(\frac{1}{4}\right) = 100\Omega$$

$$C_{T1} = \left(800\frac{af}{\mu^2}\right)\left(\frac{40\mu^2}{2}\right) = 16fF = C_{T2}$$

(assume $C_d = 800\,af/\mu^2$ for both poly layers)

$$t_{PROP}(A\to X) = 2\Big[R_{T1}C_{T1} + 3R_{T1}C_{T1} + 4R_{T1}C_1 + (4R_{T1}+R_{T2})C_{T2} + (4R_{T1}+3R_{T2})C_{T2} + (4R_{T1}+4R_{T2})C_2\Big]$$

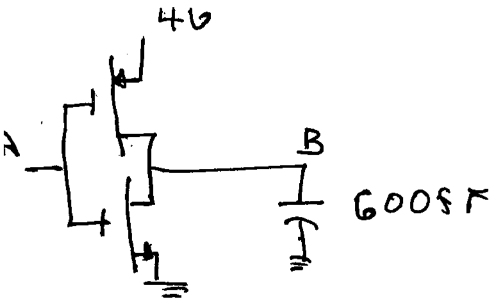
$$= 57.2\ psec$$

$$t_{PROP}(A-G) = t_{PROP}(A-X) + t_{REF}\cdot FI_G$$

$$\doteq 57.2\,psec + (20\,psec)(10)$$

$$= 257\,psec$$

8) Assume .5μ process with $W_{min} = .9\mu$, $L_{min} = .6\mu$, $C_{REF} = 4fF$



$OD_{HL} = \frac{10}{.9} = 11.1$

$OD_{LH} = \frac{40}{(3)(.9)} = 14.8$

a) $P_{dynamic} = f_{CLK} C_L V_{DD}^2 = (10^4)(600fF)(4v)^2$
$= 96nW$

b) same as part a) since load unchanged

c) $t_{PROP} = \frac{t_{REF}}{2}\left[\frac{1}{OD_{HL}} + \frac{1}{OD_{LH}}\right] FI$

$= \frac{t_{REF}}{2}\left[\frac{1}{11.1} + \frac{1}{14.8}\right]\left(\frac{600}{4}\right)$

$= 11.9\, t_{REF}$

t_{CLK} must exceed t_{PROP}

$\therefore\ t_{CLK} > 11.9\, t_{REF}$

or $f_{CLK} < \frac{1}{11.9\, t_{REF}} = \frac{1}{(11.9)(20psec)}$

$f_{CLK} < 4.2E9 = 4.2GHz$

9) The FI for a minimum sized inverter is 4fF. Total energy dissipated for charging and discharging a 4fF load is $E = CV^2 = (4fF)(16v^2) = 64fJ$

If all gates have FI = ½ and half transition on each clock cycle, dynamic power dissipated on a clock cycle would be $(500{,}000)(64fJ) = 32nJ$. If the clock frequency is 1.5 GHz $P = (32nJ)(1.5GHz) = 48W$

10) Dynamic power is independent of driver sizing

$P_{DYNAMIC} = f_{CLK} C_L V_{DD}^2 = (300MHz)(25pF)(4v)^2 = 120mW$

11) $P_{Dynamic} = \left(\frac{f_{CLK}}{2}\right)(C_L) V_{DD}^2 \cdot 32 = \left(\frac{800M}{2}\right)(4pf)(4v)^2(32) = 820mW$